In the Specification

Please replace the paragraph beginning on page 11, line 1 with the following amended paragraph:

Figure 10 shows an alternative circuitry adapted to effect the introduction of a phase lag at the second flip flop. In this embodiment only one delay element (1100) is introduced after the AND gate. The output of the delay element (1100) is input to the reset element of the second flip flop, and no delay element is introduced between the AND gate output and the reset element of the first flip flop. As such the overall effect is the same as that implemented using the circuitry of Figure 8[[,]], i.e., a time lag is introduced at the second flip flop relative to the first flip flop. Assuming that the up and dn outputs are zero, so as to effect an output current Icp as zero, the leading edge of Rclk will cause a low to high transition on "dn". When both "up" and "dn" are high the output of the AND gate will go high, resetting the "up" signal to low. A time □ later, the "dn" signal will reset to low. The timing sequence illustrated in Figure 9 is equally applicable for this embodiment, the effect on the PLL circuitry being that the loop settles into a steady state with an average phase lag on Nclk's rising edge relative to Rclk being equivalent to the amount of the delay introduced in the Nclk flip flop's reset path.